



ACM MobiCom 2026

Austin, Texas



RadioStream: A Wideband Multi-Antenna SDR Platform

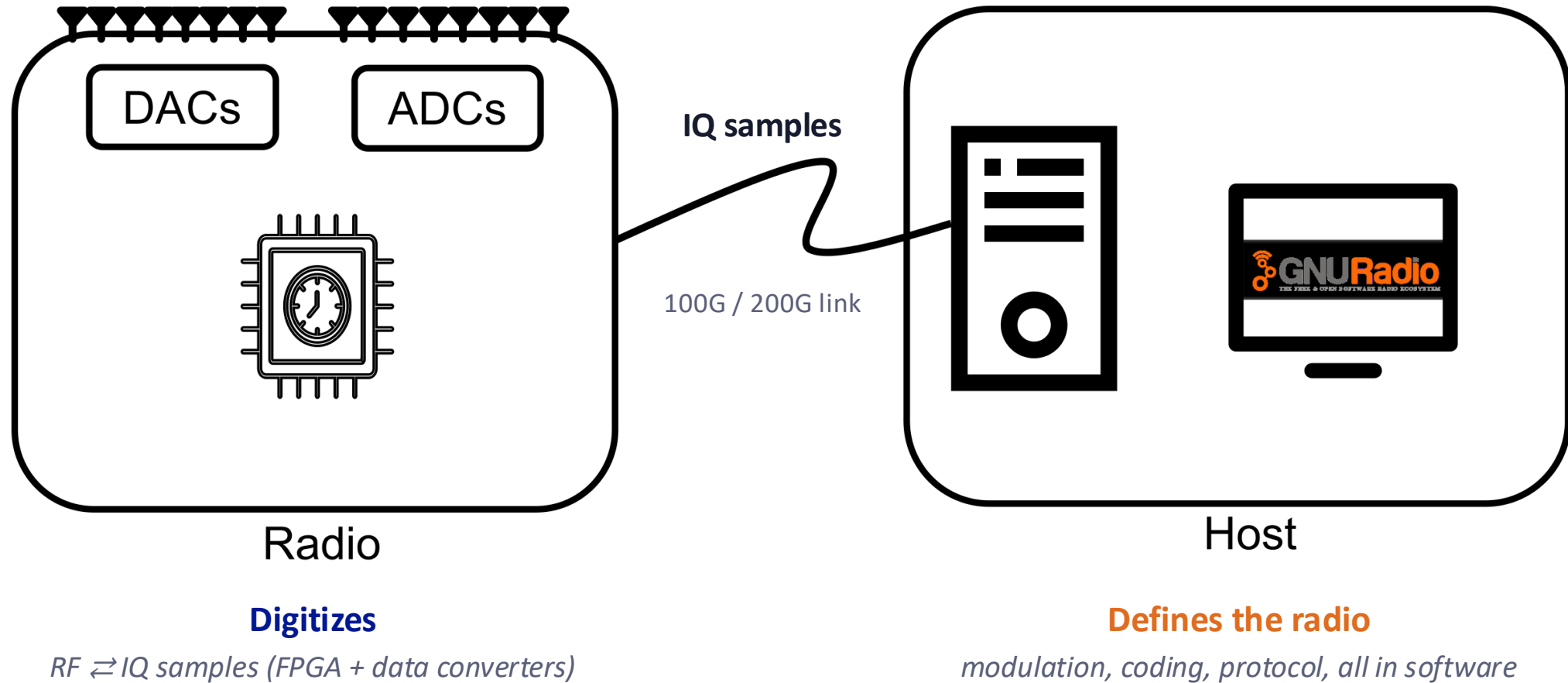
- **Adel Heidari**, University of California, San Diego

28 October 2026

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IIT Madras | UC San Diego

What is a software-defined radio (SDR)?



Hardware digitizes, software defines the radio, so every sample crosses the link.

SDRs have left the lab: they now run real networks



CELLULAR • OPEN RAN

“AT&T awards \$14 billion open RAN contract to Ericsson, dealing blow to Nokia”

Fierce Network • Dec 2023



MILITARY & DEFENCE

“IAF awards ₹275 Cr order to Hyderabad’s Astra Rafael Comsys for cutting-edge SDRs”

Indian Defence News • Jan 2026



SPACE COMMUNICATIONS

“Software-defined Eutelsat bird takes flight”

Mobile World Live • Aug 2021



SENSING & SURVEILLANCE

“Ericsson and Erillisverkot demonstrate 5G ISAC drone detection for Finnish authorities”

Ericsson • Sep 2026

Where wireless is heading next

More antennas

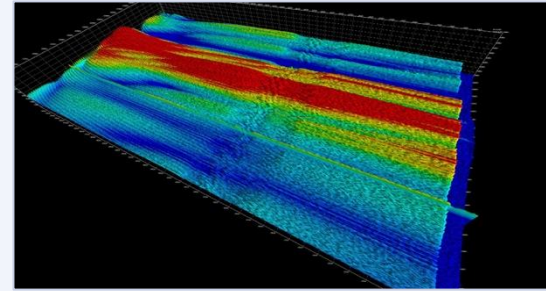


RCR Wireless · Mar 2024

4,096

antenna elements
in Qualcomm's Giga-MIMO
6G prototype: 16× today's
massive MIMO

More bandwidth



NewscastStudio · Jul 2026

440 MHz

of contiguous mid-band
the FCC “super band”; 6G
eyes the 7–24 GHz upper
mid-band next

EXAMPLE · SENSING

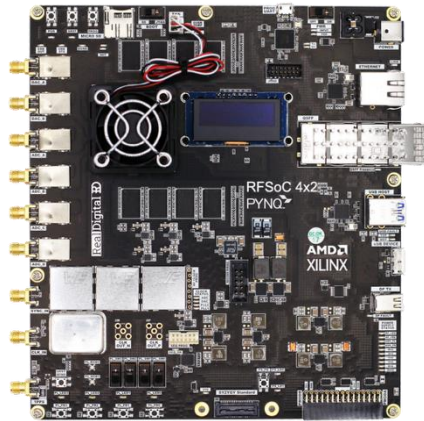
New applications need both: resolution improves directly with bandwidth and antennas

higher bandwidth → Better Range resolution

higher number of antennas → Better Angle resolution

Next-gen wireless needs SDRs with far more bandwidth and antennas.

What an SDR must deliver



Radio



Host

Wideband streaming $\leftarrow \text{antennas} \times \text{bandwidth}$

Tens of Gbps of IQ, lossless, so processing stays in host
software: **antennas** $\times$ **bandwidth** $\times$ **bits/sample**

Data to move $\propto$ antennas $\times$ bandwidth

at 491.52 MHz: 1 antenna $\approx$ 16 Gbps $\rightarrow$ 8 antennas $\approx$ 126 Gbps

16-bit I + 16-bit Q per sample

More bandwidth $\times$ more antennas means far more data

Why is this a difficult problem

RADIO (FPGA + RF front-end)

- **Deterministic and Clock driven**
- Locked to the RF sampling clock
- Keeps the exact time

≠

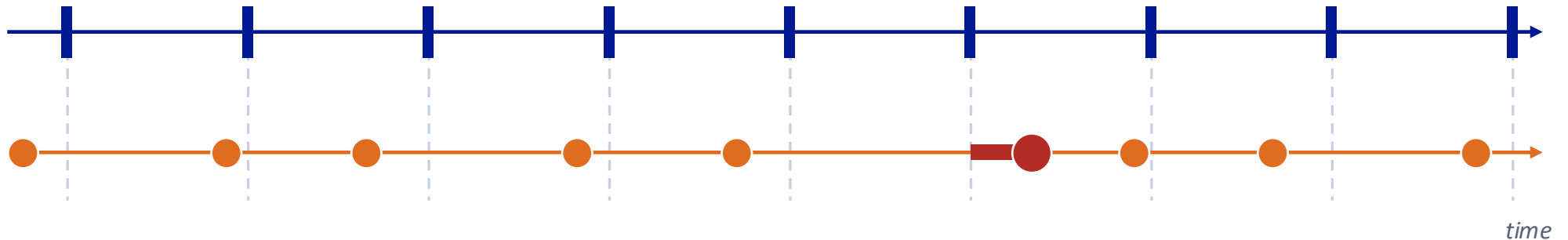
two clocks,
one timeline

HOST (x86 + Linux)

- **Non-deterministic and Software driven**
- OS scheduling, interrupts, queueing
- Has massive compute capacity, but transmission timing is highly variable

Radio
exact ticks

Host
jittered



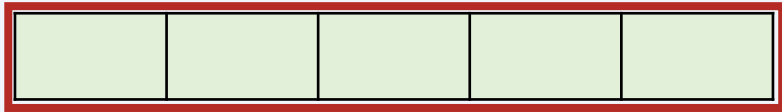
SDR must sustain a high-speed link, but only one side has a deterministic timing model

Issues with current systems

RADIO (FPGA + RF front-end)

Buffers:

Underflow!

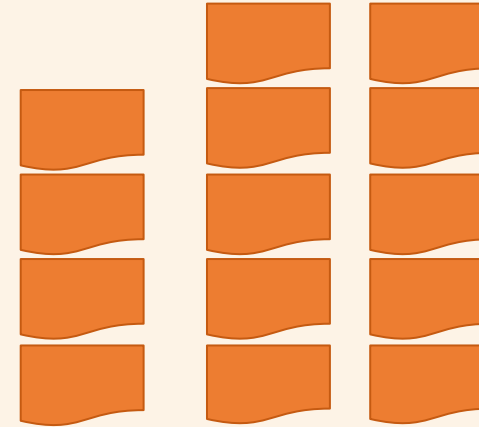


filled by the host, drained by the DAC

4

HOST (x86 + Linux)

OS stall



UUU 000000 L UUUUU 00000000 LL UUUU 00000

Host-
centric
systems

Deploy buffer
flow control
mechanisms

Loop: credits from the
FPGA
-> Host transmissions
(tight boundary)

Even a very small
context switch in the
host -> Underflow

FLIP THE SWITCH: FPGA drives the data streaming

1

FPGA owns time

A counter running on the RF sampling clock generates a tick every 0.5 ms [defined as a **SLOT**]

Generates a tick with SLOT NUMBER every 0.5 ms

2

Host programs the future

On reception of tick, it sends configuration and/or samples labelled for the upcoming slot.

two-slot look-ahead

3

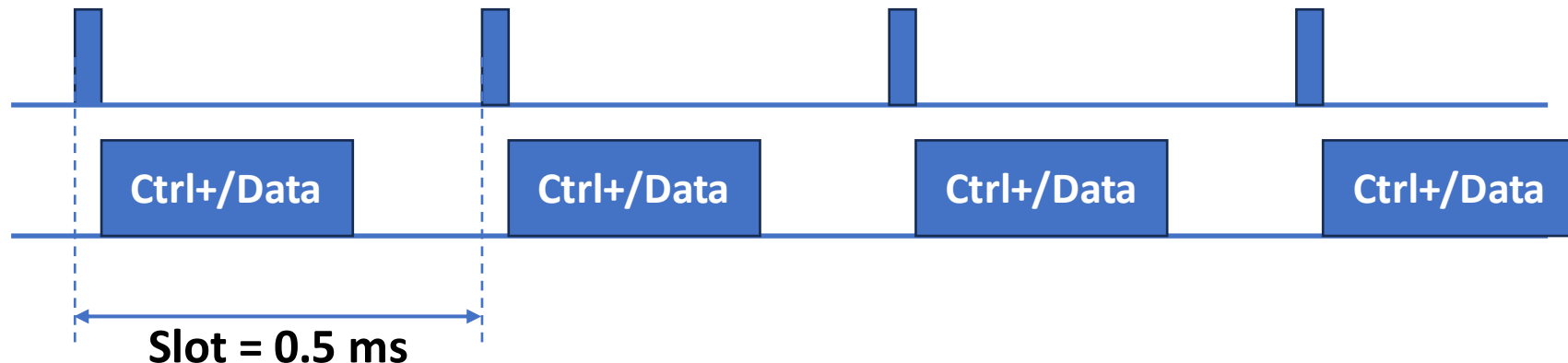
FPGA commits at the boundary

IQ samples are held in a buffer, transferred only when the counter reaches that slot.

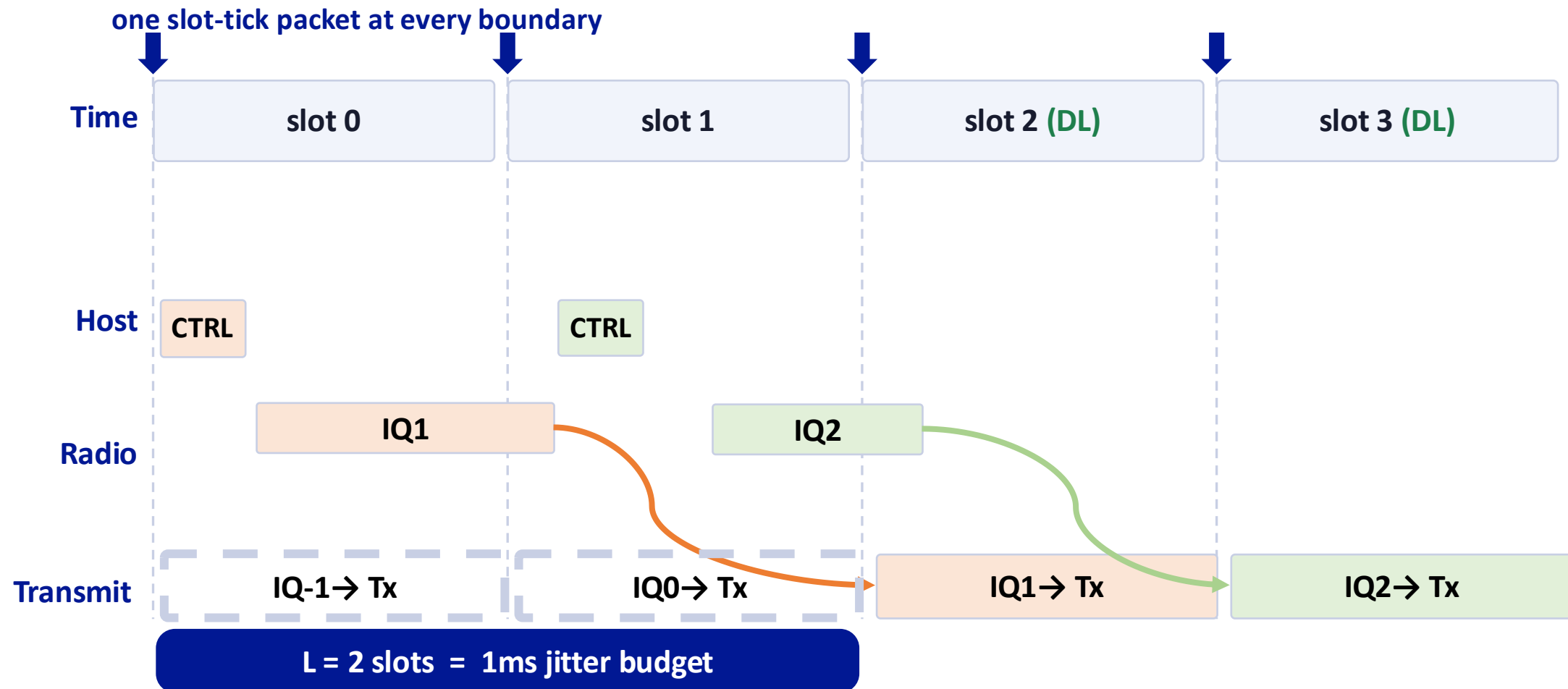
slot-indexed PL-DDR4 buffers

FPGA exposes Slot Tick

Host PC Processing

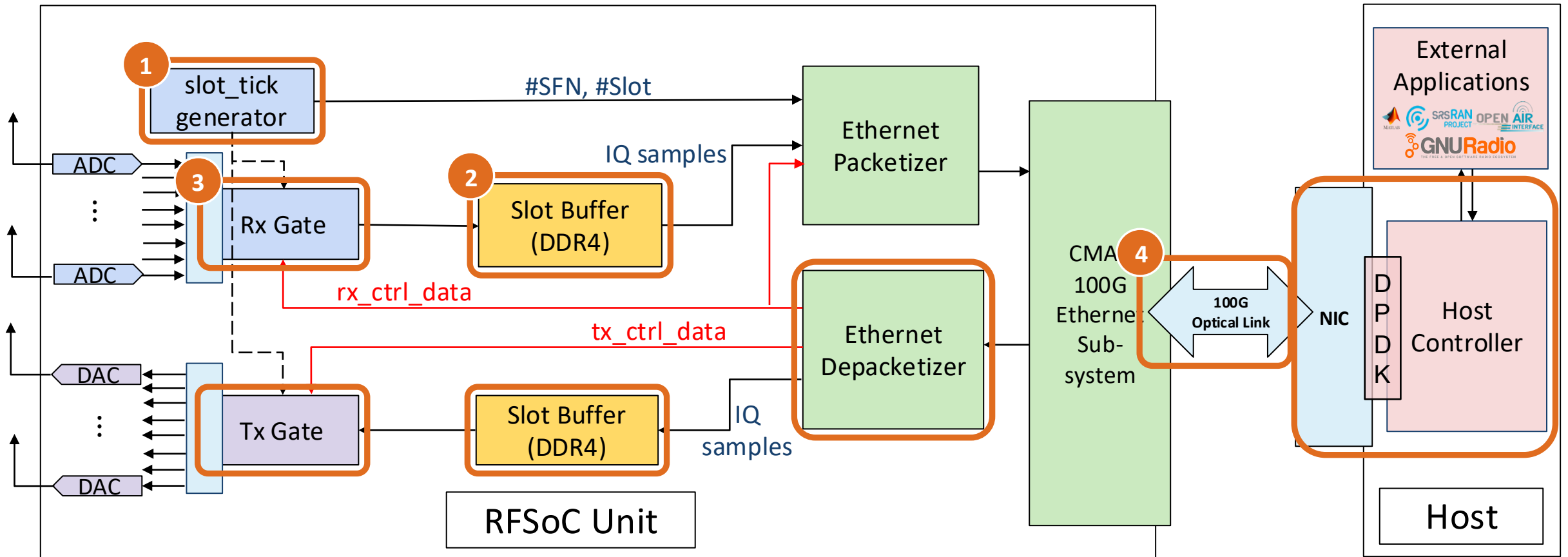


System timing: Two slots look-ahead, commits at the boundary

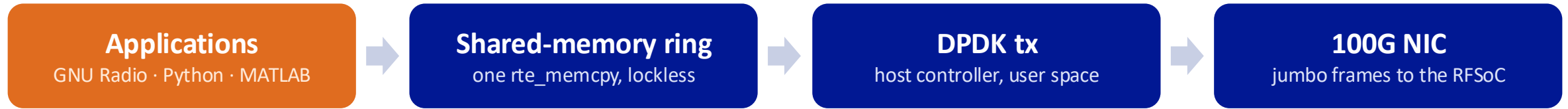


The host never races a deadline - it labels its intent, and the FPGA decides when that intent becomes real.

RadioStream architecture



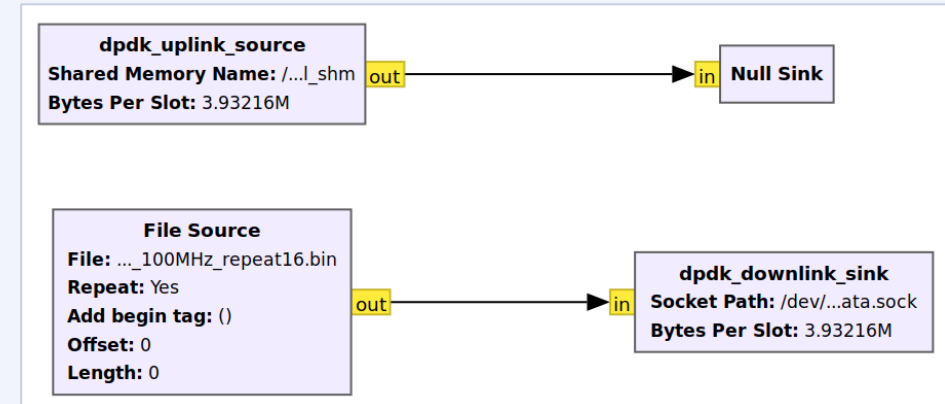
Host side: just one memory copy from GNU Radio to the NIC



All the host has to do

- 1 memory copy**
shared ring → NIC, one vectorized memcpy
- 0 flow control**
no credits, no ACKs: the radio already owns time
- 3 CPU cores for 98 Gbps**
zero kernel copies, zero syscalls

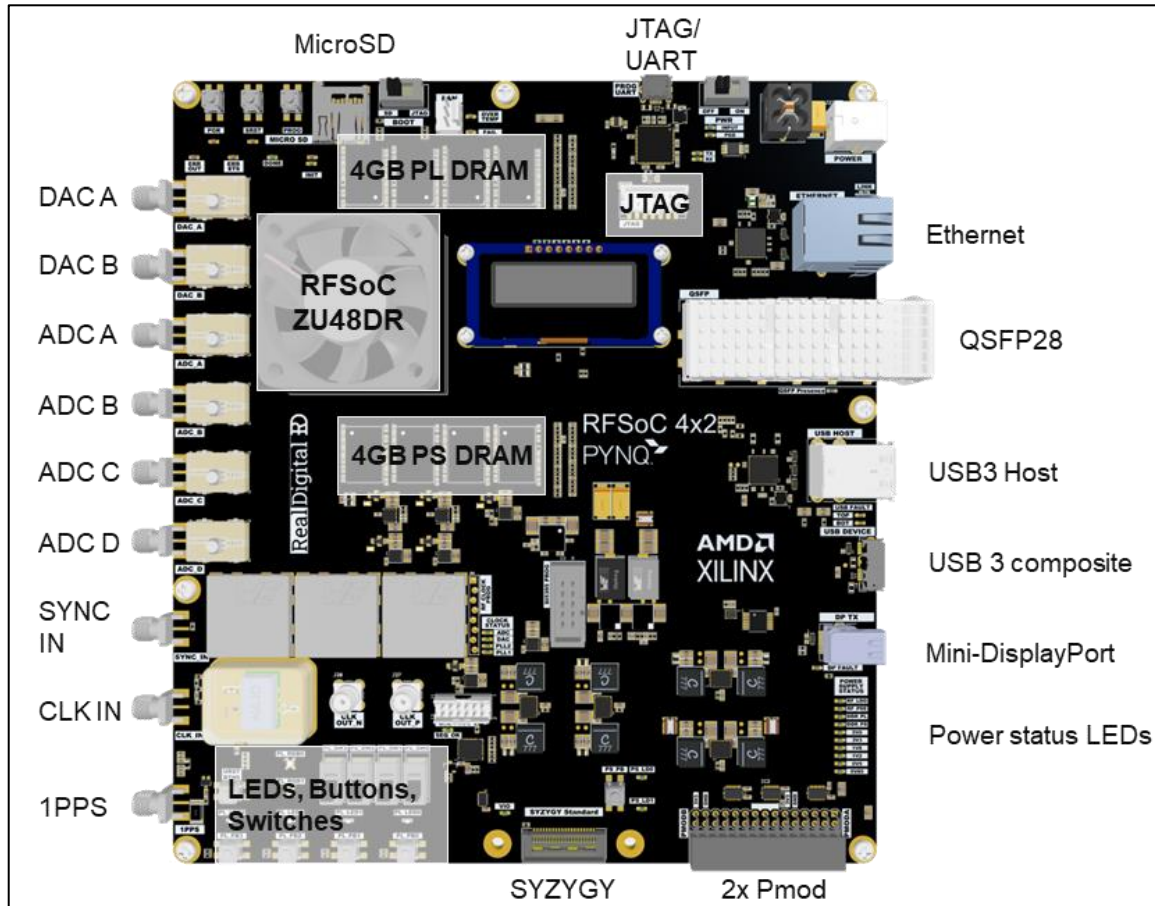
Plugs straight into GNU Radio



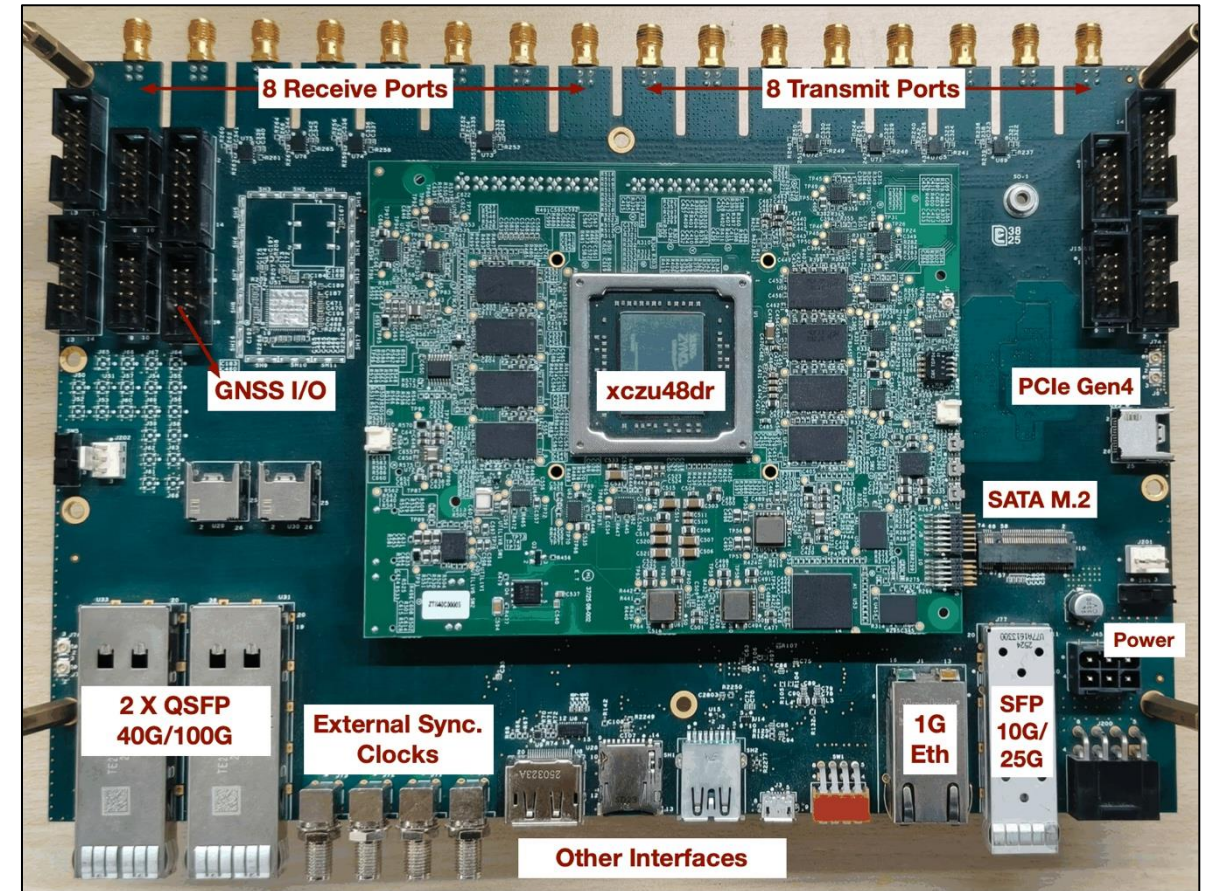
OOT blocks map the ring with zero copies
No DPDK dependency inside GNU Radio
GNU Radio stalls never touch the radio link

The radio owns time, so the host just copies

Implementation



(a)



(b*)

Implemented and tested the design on **(a)** RFSoc 4x2 (4 ADC / 2 DAC) and **(b)** a custom 8T8R SOM, both XCZU48DR. Host is verified with both Mellanox ConnectX-5 and Intel E810 - the result reproduces on both.

*The custom SOM + RF Carrier boards are developed by REIO Systems Pvt. Ltd., India

Throughput and transport latency

transport time for one slot (μs) / instantaneous throughput (Gbps), 5-hour average.

BW	1 ch ($\mu\text{s}/\text{Gbps}$)	2 ch ($\mu\text{s}/\text{Gbps}$)	4 ch ($\mu\text{s}/\text{Gbps}$)	8 ch ($\mu\text{s}/\text{Gbps}$)
122.88 MHz	19.98 / 98.4	39.82 / 98.8	79.60 / 98.8	159.3 / 98.7
245.76 MHz	39.81 / 98.8	79.59 / 98.8	159.3 / 98.8	346.6 / 90.8
491.52 MHz	79.59 / 98.8	159.3 / 98.7	345.7 / 91.0	-

~2 GHz

max aggregate RF BW

90-100 Gbps

sustained on the link

0

drops in 5-hour testing

3 cores

in the host controller

Uplink reliability against a commercial baseline

Aggregate uplink rate	USRP X410 + UHD 4.8	RadioStream
491.52 Msps	lossless	lossless
983.04 Msps (2 × 491.52)	0.0047% lost	0 samples lost
1966.08 Msps (4 × 491.52)	Fails with single 100G QSFP link	rate sustained, on 3 cores with single 100G QSFP link

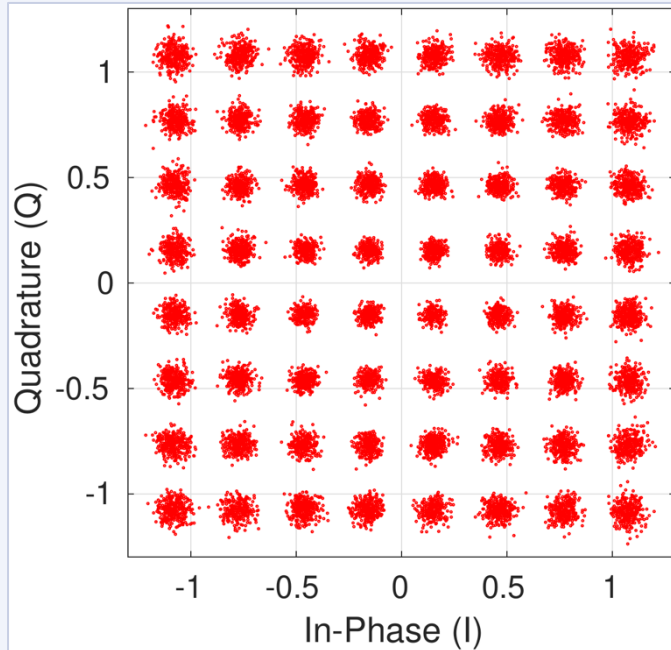
Where do the samples go?

- **The X410 Limit:** Even with 8 dedicated cores, transport link lost samples. It could be due to buffering or insufficient number of cores.
- **The RadioStream Advantage 1 (Buffering):** PL-DDR4 provides a larger jitter budget. When the exact same OS stall happens, the deep memory absorbs it. The host catches up, and zero samples are lost.
- **The RadioStream Advantage 2 (Efficiency):** No flow-control, the transport is just a simple memory pipe. The system easily sustains the rate on just 3 cores.

Three applications, end to end

APPLICATION 1 · 491.52 MHz OTA

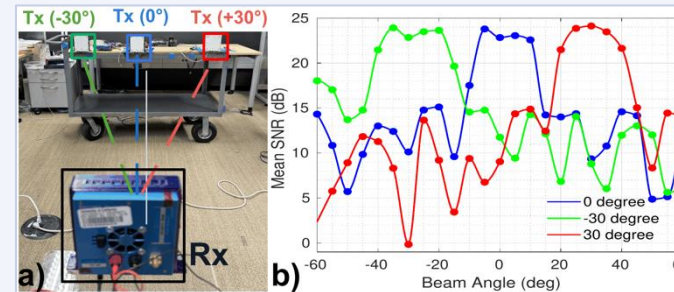
Wideband communication



64-QAM over the air; every slot on time.

APPLICATION 2 · 491.52 MHz

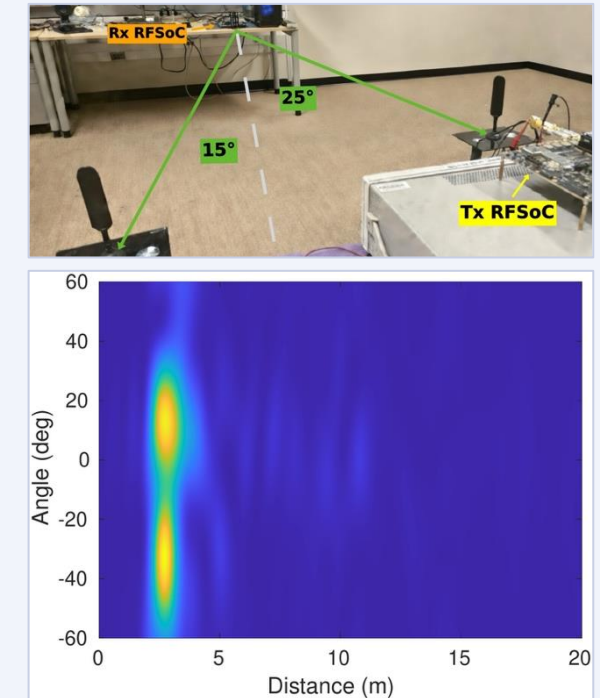
28 GHz beam sweeping



Per-slot steering; peaks hit all 3 Tx angles.

APPLICATION 3 · 4 antennas, 491.52 MHz

AoA + range sensing



Coherent channels resolve angle + range.

Real applications, end to end: **wideband, multi-antenna IQ streamed straight to software.**

Takeaways

Exported radio time

The FPGA is the sole authority and ships its time to the host as a packet.

p99 jitter 598 ns

Slot-addressable control and data

Slot-tick, control and IQ are three separate, slot-addressable classes;

90 Gbps, 0 drops

Buffering

IQ samples are transferred two slots early and buffered in the FPGA to mask OS jitter

Two slot look-ahead notion

Limitations and what's next

- **Scaling past one link.** 8 ch × 491.52 MHz full-duplex is ≈126 Gbps; the second QSFP is already routed.
- **Full-stack integration.** srsRAN / OAI via a thin adapter - no FPGA or DPDK fast-path changes.
- **Multi-node sync.** The contract extends over a shared GPS/PTP reference; still open.

Thank you!

Questions?

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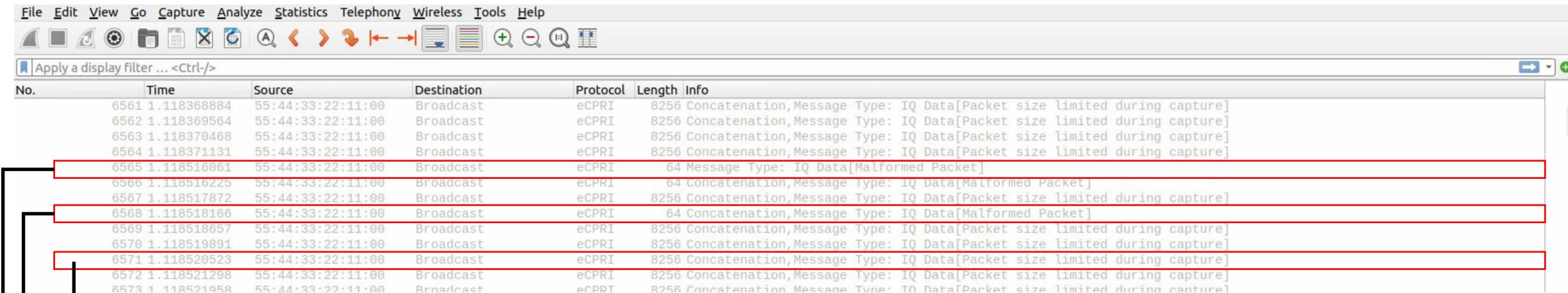


Paper & project page
wcsng.ucsd.edu/radiostream



My website
adheidari.github.io

Three kinds of raw Ethernet packets on one link

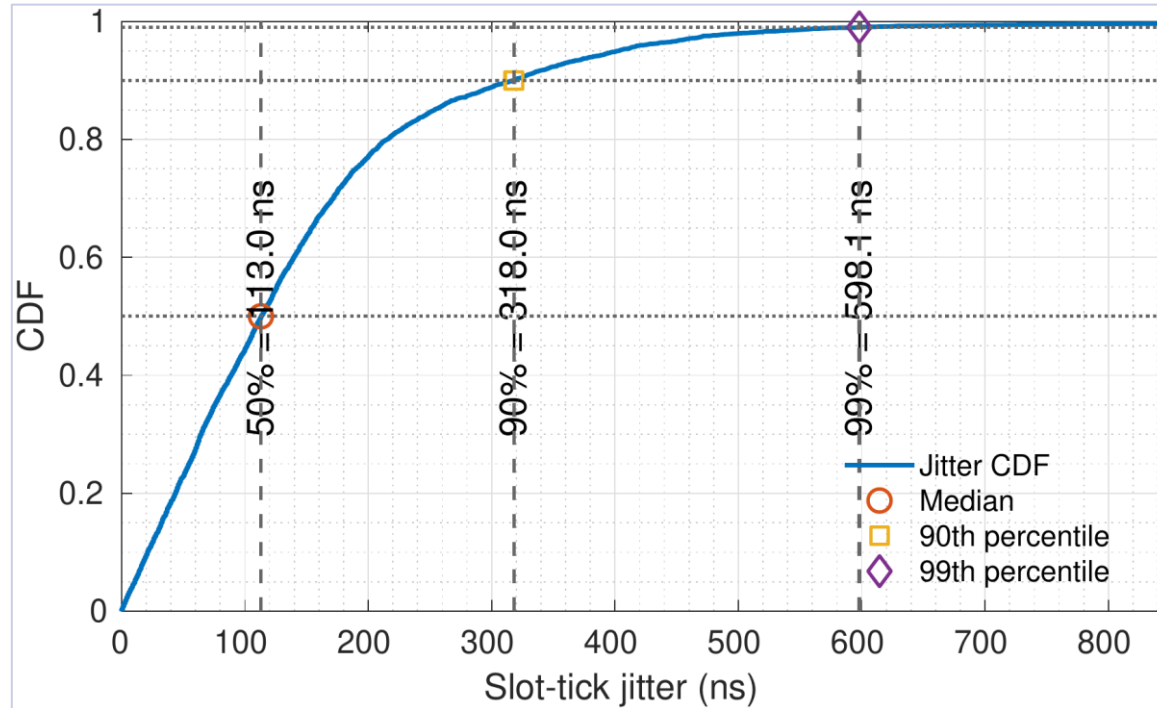


No.	Time	Source	Destination	Protocol	Length	Info
6561	1.118368884	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6562	1.118369564	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6563	1.118370468	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6564	1.118371131	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6565	1.118516061	55:44:33:22:11:00	Broadcast	eCPRI	64	Message Type: IQ Data[Malformed Packet]
6566	1.118516225	55:44:33:22:11:00	Broadcast	eCPRI	64	Concatenation, Message Type: IQ Data[Malformed Packet]
6567	1.118517872	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6568	1.118518166	55:44:33:22:11:00	Broadcast	eCPRI	64	Concatenation, Message Type: IQ Data[Malformed Packet]
6569	1.118518657	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6570	1.118519891	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6571	1.118520523	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6572	1.118521298	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]
6573	1.118521958	55:44:33:22:11:00	Broadcast	eCPRI	8256	Concatenation, Message Type: IQ Data[Packet size limited during capture]

Packet type	Direction	Size	Carries
Slot tick	FPGA -> Host	64 B	Current slot number. Exports radio time.
Data	Host -> FPGA (D) FPGA -> Host (U)	9000 B MTU	Uplink / downlink IQ, tagged (slot, direction).
Control	Host -> FPGA	64 B	Antennas, direction, NCO frequency, NCO phase.

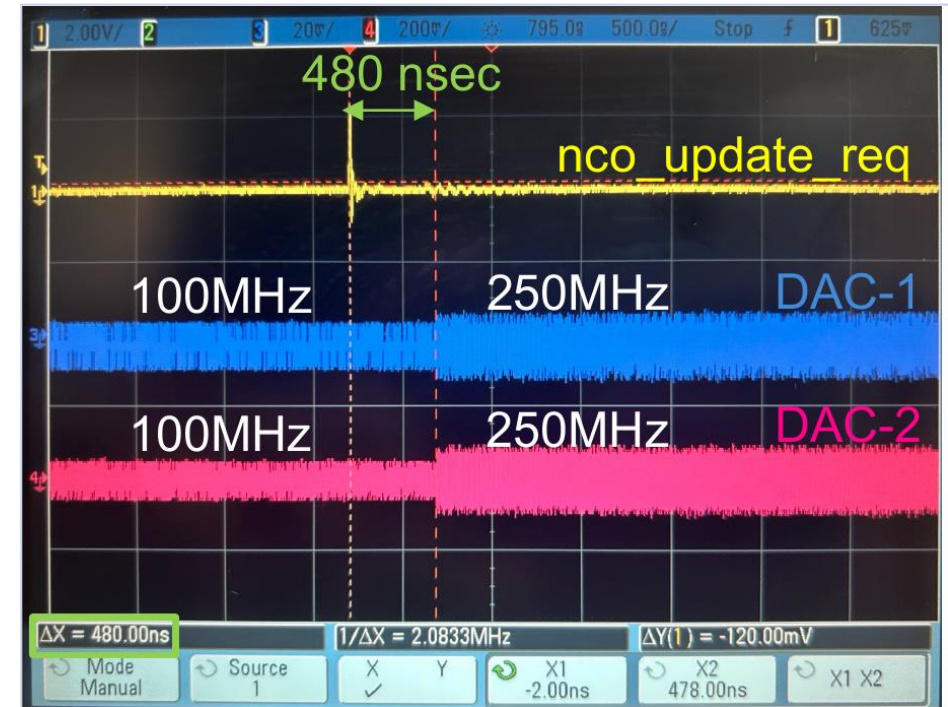
Timing accuracy and control latency

How accurately does the host see radio time?



median 113 ns | p90 318 ns | p99 598 ns

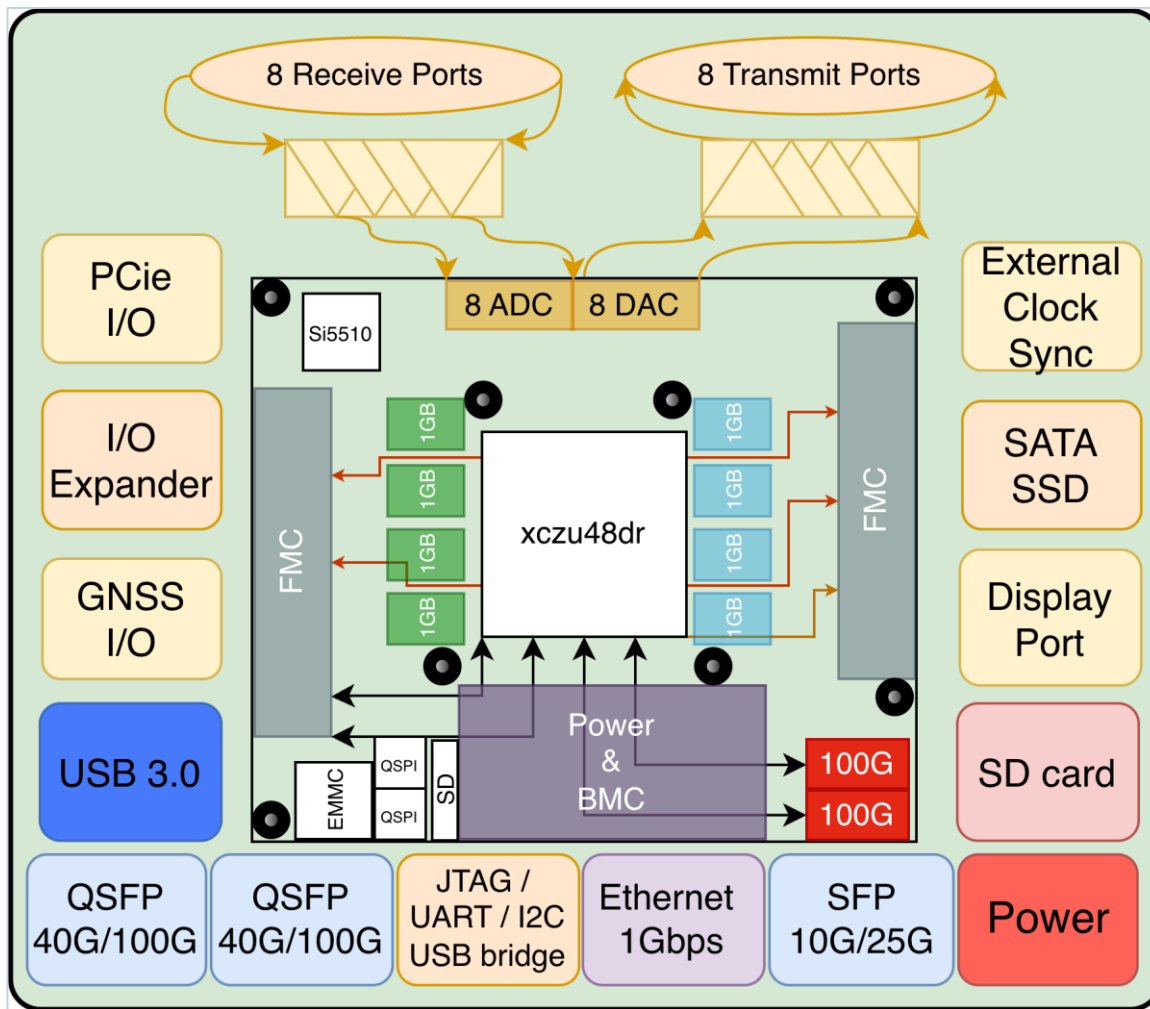
How fast does RF control command reach the air?



480 ns end-to-end - of which the RFDC update is 360 ns

Sub- μs on both sides: the host follows radio time to $\sim 0.6 \mu\text{s}$, and control lands at the RF output in under $0.5 \mu\text{s}$.

The SOM and RF carrier board



System-on-Module

- **xczu48dr** - 8 ADC to 5 GSps and 8 DAC to 9.85 GSps, each through its own gain stage.
- **4 GB of DDR4 on the FPGA side** - this is where the slot buffers live.
- **Two 100 Gb ports** - we use one. The second is the headroom for 8 channels at full width.

RF carrier board

- Breaks out all 16 RF chains, both QSFP28 cages, PCIe x8, GPS in and management Ethernet.

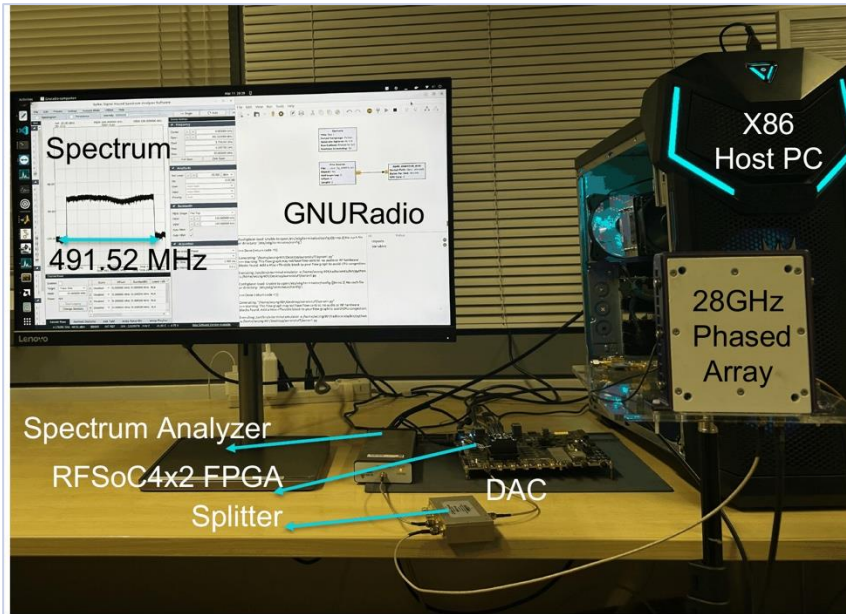
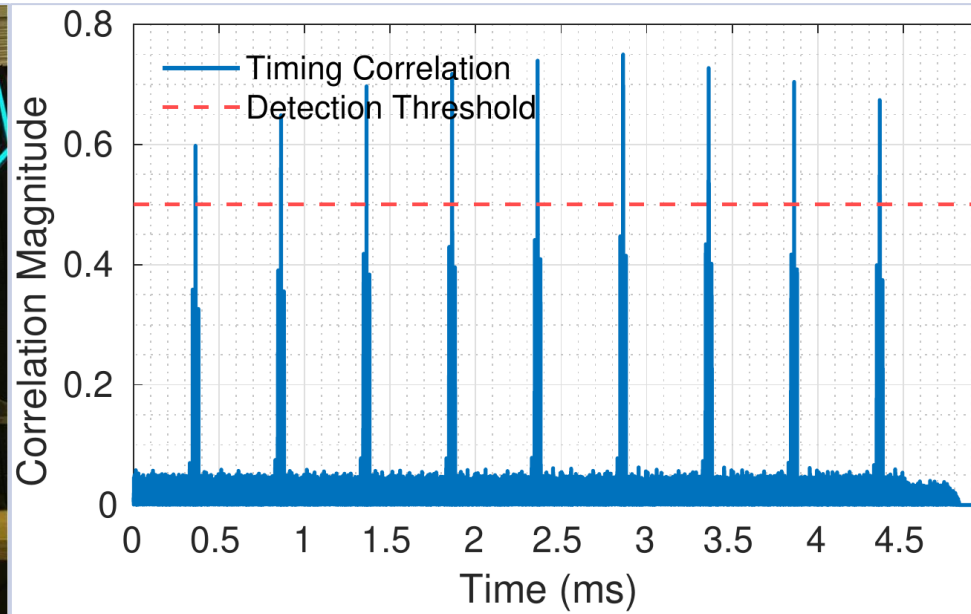
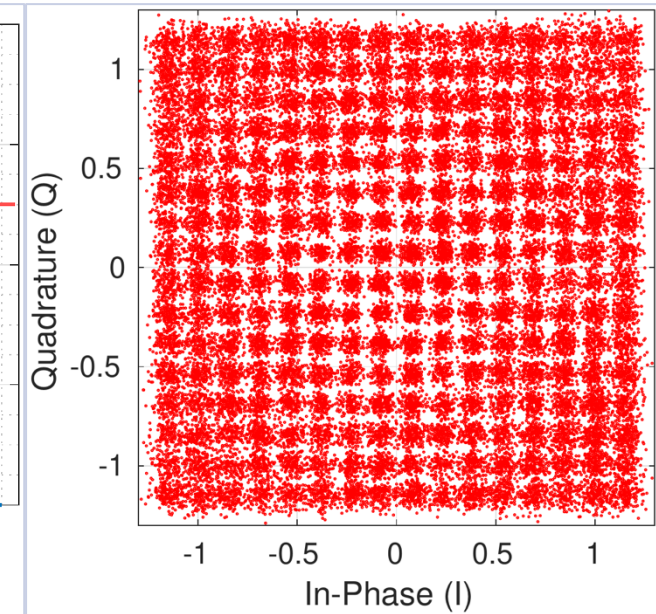
8T8R
transmit / receive

2 × 100G
Ethernet ports

4 GB
PL-side DDR4

One shared clock (GPS or PTP) drives every converter, so all channels stay phase-coherent.

Application 1: Wideband Communication



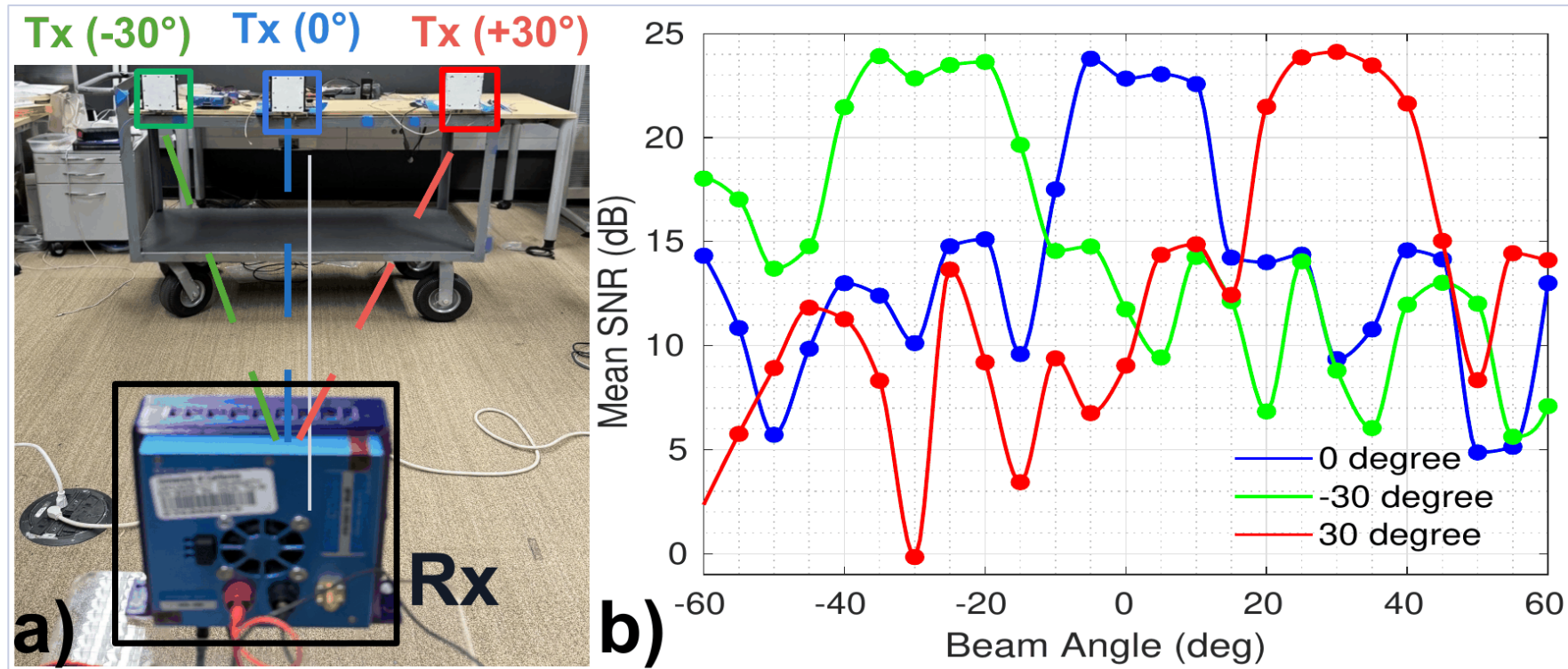
5G-style OFDM waveform

256-QAM
491.52 MHz IBW @ $f_c = 28$ GHz

EVM 4-6%
flat across slot and resource block

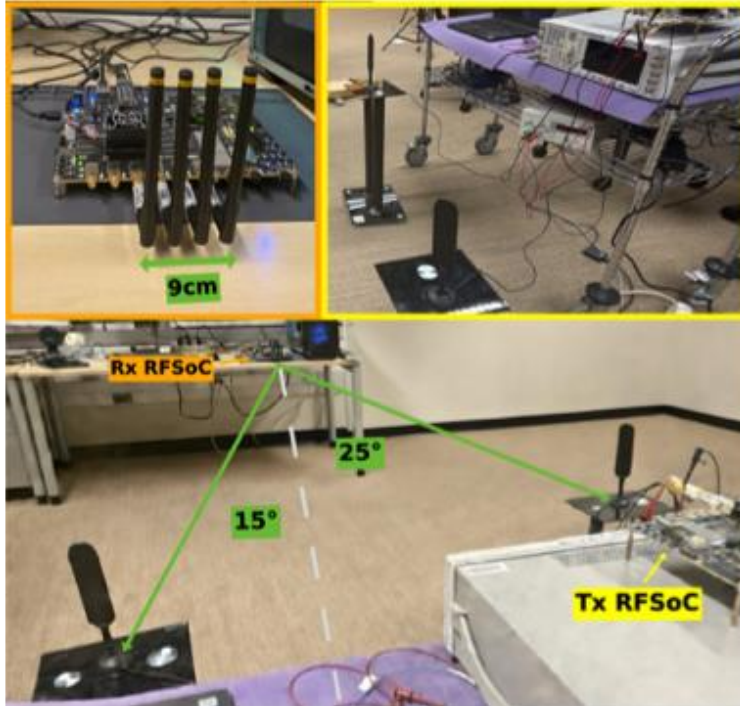
Lossless 491.52 MHz streaming over the air: every slot on time, 256-QAM at 4–6% EVM.

Application 2: 28 GHz mmWave beam sweeping

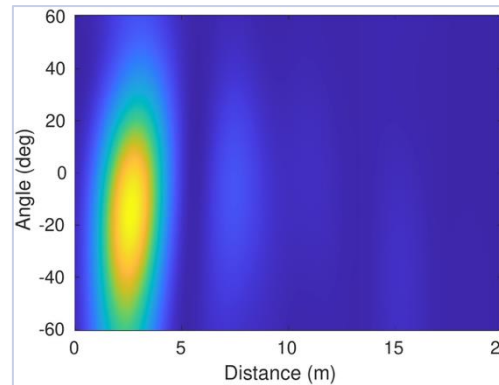


- RFSoc sweeps the beam while streaming continuously at 491.52 MHz.
- Peaks land on the three known transmitter angles.
- Steering happens per slot, on the wire already carrying the samples.

Application 3: WiFi AoA and range estimation

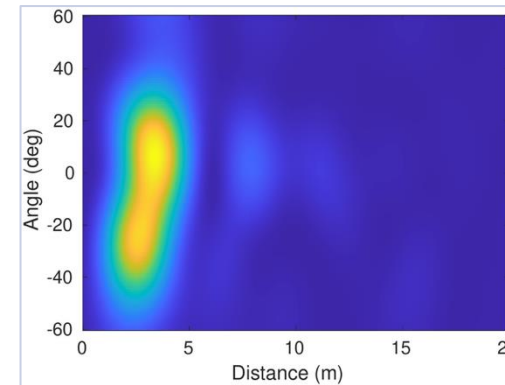


Setup: Two sources at 4 GHz;
receive elements 3 cm apart.



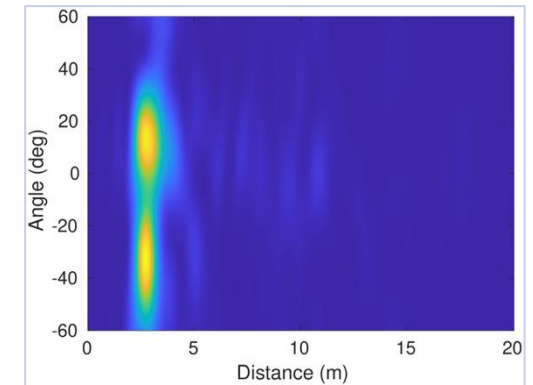
122.88 MHz · 2 antennas

the two sources merge



122.88 MHz · 4 antennas

angle resolves: 40° → 20°



491.52 MHz · 4 antennas

range resolves: 2.4 m → 0.6 m

Bandwidth buys range, antennas buy angle.

4 phase-coherent antennas at 491.52 MHz, streamed live, resolve both angle and range.

Throughput and transport latency

transport time for one slot (μs) / instantaneous throughput (Gbps), 5-hour average.

orange = limited by the memory path, not the 100G link

BW	Path	1 channel ($\mu\text{s}/\text{Gbps}$)	2 channel ($\mu\text{s}/\text{Gbps}$)	4 ch ($\mu\text{s}/\text{Gbps}$)	8 ch ($\mu\text{s}/\text{Gbps}$)
122.88 MHz	FPGA $\leftrightarrow$ Host	19.98 / 98.4	39.82 / 98.8	79.60 / 98.8	159.3 / 98.7
	Host $\leftrightarrow$ App	15.11 / 130	30.09 / 131	59.88 / 131	120.2 / 131
245.76 MHz	FPGA $\leftrightarrow$ Host	39.81 / 98.8	79.59 / 98.8	159.3 / 98.8	346.6 / 90.8
	Host $\leftrightarrow$ App	29.97 / 131	59.81 / 131	120.4 / 131	294.1 / 107
491.52 MHz	FPGA $\leftrightarrow$ Host	79.59 / 98.8	159.3 / 98.7	345.7 / 91.0	-
	Host $\leftrightarrow$ App	59.88 / 131	120.2 / 131	295.8 / 106	-

~2 GHz

max aggregate RF BW

90-100 Gbps

sustained on the link

0

drops in 5-hour testing

3 cores

in the host controller